IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A microelectronic device comprising:

a microelectronic die having a plurality of bond pads on an active surface thereof, said microelectronic die being fixed within an opening in a package core; and

an interfacial metal layer deposited over said active surface of said microelectronic die, said interfacial metal layer having at least one single conductive element that is conductively coupled to multiple bond pads on said active surface of said microelectronic die to provide signal distribution between points within said microelectronic die.

2. (Original) The microelectronic device of claim 1, comprising:

at least one build up metallization layer deposited over said interfacial metal layer, said at least one build up metallization layer being conductively coupled to said interfacial metal layer through a dielectric layer having a plurality of via holes.

3. (Currently Amended) The microelectronic device of claim 1, wherein:

said at least one single conductive element includes a first pad that is directly coupled to a first bond pad on said active surface of said microelectronic die, a second pad that is directly coupled to a second bond pad on said active surface of said microelectronic die, and a conductive trace portion connecting said first and second pads.

4. (Currently Amended) The microelectronic device of claim 1, wherein:

said at least one single conductive element is configured to receive a signal from a first bond pad on said active surface of said microelectronic die to transfer said signal to a second bond pad on said active surface of said microelectronic die.

5. (Previously Presented) The microelectronic device of claim 4, wherein:

said microelectronic die includes a clock source to provide a clock signal to a first bond pad on said active surface, wherein said interfacial metal layer includes a conductive element that is conductively coupled to said first bond pad and to a plurality of other bond pads on said active surface to distribute said clock signal to said plurality of other bond pads.

6. (Original) The microelectronic device of claim 1, wherein:

said package core is formed from a metal material.

7. (Original) The microelectronic device of claim 1, wherein:

said interfacial metal layer is deposited on a passivation layer of said microelectronic die.

8. (Original) The microelectronic device of claim 1, comprising:

a second microelectronic die fixed within said package core, wherein said interfacial metal layer includes at least one conductive element that is conductively coupled to both a first bond pad on said active surface of said first microelectronic die and a second bond pad on an active surface of said second microelectronic die.

9. (Original) The microelectronic device of claim 1, wherein:

said microelectronic die is fixed within said opening in said package core using an encapsulation material.

10. (Currently Amended) A microelectronic device comprising:

at least one microelectronic die having a plurality of bond pads on an active surface thereof and a passivation layer covering said active surface, said passivation layer having a plurality of openings in locations corresponding to said plurality of bond pads, said at least one microelectronic die being fixed within a package core; and

an interfacial metal layer over said passivation layer, said interfacial metal layer having a plurality of separate conductive elements including at least one separate conductive element that

is conductively coupled to multiple bond pads on said at least one microelectronic die through corresponding openings in said passivation layer.

11. (Currently Amended) The microelectronic device of claim 10, wherein:

said at least one separate conductive element on said interfacial layer is configured to receive a signal from a first of said multiple bond pads to distribute said signal to each other of said multiple bond pads.

12. (Currently Amended) The microelectronic device of claim 10, wherein:

said at least one separate conductive element on said interfacial layer is conductively coupled to a first external contact of said microelectronic device through said metallization layer.

13. (Currently Amended) The microelectronic device of claim 12, wherein:

said at least one separate conductive element on said interfacial layer is configured to receive a signal from said first external to distribute said signal to said multiple bond pads in response thereto.

14. (Currently Amended) The microelectronic device of claim 10, wherein:

said at least one microelectronic die includes a first microelectronic die and a second microelectronic die, wherein said at least one separate conductive element on said interfacial layer is conductively coupled to both a first bond pad on said first microelectronic die and a second bond pad on said second microelectronic die.

15. (Currently Amended) The microelectronic device of claim 14, wherein:

said at least one separate conductive element on said interfacial layer is configured to receive a signal from said first bond pad on said first microelectronic die to deliver said signal to said second bond pad on said second microelectronic die.

16. (Original) The microelectronic device of claim 10, wherein:

said interfacial metal layer includes a first portion overlapping said at least one microelectronic die and a second portion overlapping said package core.

17. (Original) The microelectronic device of claim 10, comprising:

a dielectric layer deposited on said interfacial metal layer, said dielectric layer having a plurality of via holes in locations corresponding to selected conductive elements on said interfacial metal layer.

18. (Original) The microelectronic device of claim 17, comprising:

a metallization layer deposited on said dielectric layer, said metallization layer having conductive elements that are conductively coupled to said selected conductive elements of said interfacial metal layer through said plurality of via holes in said dielectric layer.

19. (Original) The microelectronic device of claim 18, wherein:

said metallization layer includes a first portion overlapping said at least one microelectronic die and a second portion overlapping said package core.

20. (Currently Amended) A microelectronic device comprising:

a package core;

a first microelectronic die fixed within said package core, said first microelectronic die having bond pads on an active surface thereof;

a second microelectronic die fixed within said package core, said second microelectronic die having bond pads on an active surface thereof; and

an interfacial metal layer deposited over said first and second microelectronic dice, said interfacial metal layer having a first single conductive element that is conductively coupled to multiple bond pads on said first microelectronic die and to both a first bond pad on said first microelectronic die and a second bond pad on said second microelectronic die.

21. (Currently Amended) The microelectronic device of claim 20, wherein:

said first single conductive element is conductively coupled to multiple bond pads on said second microelectronic device.

22. (Currently Amended) The microelectronic device of claim 20, wherein:

said first single conductive element has a first portion on a passivation layer of said first microelectronic die and a second portion on a passivation layer of said second microelectronic die.

23. (Original) The microelectronic device of claim 20, wherein:

said first and second microelectronic dice are fixed within a common opening in said package core.

24. (Original) The microelectronic device of claim 20, wherein:

said first and second microelectronic dice are each fixed within a separate opening in said package core.

25. (Original) The microelectronic device of claim 20, wherein:

said first and second microelectronic dice are fixed within said package core using an encapsulation material.

26. (Currently Amended) The microelectronic device of claim 20, wherein:

said first microelectronic die includes a signal source to provide a signal to said first bond pad, wherein said first single conductive element of said interfacial metal layer is configured to transfer said signal from said first bond pad to said second bond pad.